Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A data log acquisition circuit for acquiring a data log in correspondence with a test pattern in a test by using an IC tester, comprising:

a number-of-patterns output section ~~adapted~~ to count a number of an executed test pattern and output a count value thereof;

an identity signal output section ~~adapted~~ to compare one of an address of the test pattern and the count value with a predetermined reference value and output an identity signal when the one of the address and the number of the executed test pattern and the predetermined reference value are data for the same test pattern;

an output flag control section ~~adapted~~ to control an output flag on a basis of setting of an operation mode when the identity signal outputted by the identity signal output section is inputted;

a write address output section ~~adapted~~ to generate and output a write address of the data log when the output flag is inputted by the output flag control section;

a data log output section ~~adapted~~ to output the data log at a timing adjusted for writing the address of the test pattern as a data log; and

a storage section ~~adapted~~ to store the data log outputted by the data log output section together with the write address inputted from the address output section,

wherein, during operation, when the operation mode is in a first state, the data log is acquired from a range of test pattern addresses so as to include an address at which a FAIL signal is generated, and when the operation mode is in a second state, the data log is acquired for all test pattern addresses in the range.

2. (Currently amended) The data log acquisition circuit according to claim 1, further comprising:

a held data output section ~~adapted~~ to hold the data log and the write address to be stored in the storage section temporarily to output the data log and the write address; and

a number-of-FAIL-signals output section ~~adapted~~ to count and output the number of FAIL signal when the FAIL signal is generated.

3. (Currently amended) The data log acquisition circuit according to claim 2, wherein the held data output section further including:

a control flag output section ~~adapted~~ to output a control flag when the FAIL signal is generated; and

a clock signal mask section ~~adapted~~ to output a clock signal masked with the control flag outputted by the control flag output section,

wherein the held data output section holds the data log and the write address in synchronism with the clock signal outputted by the clock signal mask section.

4. (Currently amended) A data log acquisition method in a data log acquisition circuit for acquiring a data log in correspondence with a test pattern in a test by using an IC tester, comprising ~~the steps of~~ :

counting a number of an executed test pattern;

outputting the counted value;

comparing one of an address of the test pattern and the counted value with a predetermined reference value;

outputting an identity signal when the one and the predetermined reference value are data for the same test pattern;

controlling an output flag on a basis of setting of an operation mode when the identity signal is outputted;

generating and outputting a write address of the data log when the output flag is outputted;

outputting the data log at a timing adjusted for writing the address of the test pattern as a data log; and

storing the data log outputted together with the write address outputted,

wherein, when the operation mode is in a first state, the data log is acquired from a limited range of test pattern addresses so as to include an address at which a FAIL signal is generated, and when the operation mode is in a second state, the data log is acquired for all test pattern addresses in the range.

5. (Currently amended) The data log acquisition method according to claim 4, further comprising ~~the steps of~~:

outputting the data log and the write address to be stored after holding the data log and the write address temporarily; and

counting and outputting the number of a FAIL signal when the FAIL signal is generated.

6. (Currently amended) The data log acquisition method according to claim 5, further comprising ~~the steps of~~:

outputting a control flag when the FAIL signal is generated; and

outputting a clock signal masked with the control flag,

wherein the said data log and said write address are held in synchronism with the clock signal.